

**CLAIMS**

1. A limiter circuit formed on a semiconductor integrated circuit substrate, comprising:

5           a differential amplification circuit comprising an MIS field-effect transistor in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, terminated hydrogen on the  
10       silicon surface is removed in plasma atmosphere of an inert gas, then a gate insulating film is formed on at least a part of a top surface and the side surface of the projecting portion at a temperature at or lower than about 550°C in the plasma atmosphere, a gate is formed  
15       on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion.

2. The limiter circuit according to claim 1, wherein

20           a channel is formed on the first crystal surface of the top surface and the second crystal surface of the side surface of the projecting portion, and a channel width of the MIS field-effect transistor is at least a total of channel widths on the top surface and the  
25       side surface.

3. The limiter circuit according to claim 1 or 2,  
wherein

the projecting portion has the top surface  
5 comprising a silicon surface (100), a side surface  
comprising a silicon surface (110), and the source and  
drain are formed on the projecting portion enclosing  
the gate and in left and right areas of the projecting  
portion of the silicon substrate.

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4. The limiter circuit according to claim 1 or 2,  
wherein

the limiter circuit comprises a p-channel MIS  
field-effect transistor and n-channel MIS field-effect  
15 transistor, and a gate width of a top surface and a side  
surface of a projecting portion of the p-channel MIS  
field-effect transistor is set such that current drive  
capability of the p-channel MIS field-effect transistor  
can be substantially equal to current drive capability  
20 of the n-channel MIS field-effect transistor.

5. The limiter circuit according to claim 1 or 2,  
wherein

the limiter circuit comprises first and second MIS  
25 field-effect transistors forming a differential

amplification circuit for receiving an FM-modulated signal at a gate, and a third MIS field-effect transistor forming a constant current circuit commonly connected to a source or a drain of the first and second MIS field-effect transistors.

6. A semiconductor integrated circuit comprising on a same circuit substrate:

a circuit comprising a p-channel MIS field-effect transistor and an n-channel MIS field-effect transistor in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, terminated hydrogen on the silicon surface is removed in plasma atmosphere of an inert gas, then a gate insulating film is formed on at least one of the top surface and the side surface of the projecting portion at a temperature at or lower than about 550°C in the plasma atmosphere, a gate is formed on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion; and

a limiter circuit comprising a differential amplification circuit having the p-channel MIS field-effect transistor or the n-channel MIS

field-effect transistor.

7. The semiconductor integrated circuit according to claim 6, wherein

5 gate widths of the top surface and the side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to  
10 current drive capability of the n-channel MIS field-effect transistor.

8. The semiconductor integrated circuit according to claim 6 or 7, wherein

15 the limiter circuit comprises a CMOS circuit having the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor.